Philippe LUC
NICE, FRANCE

45 years old, Married, 2 happy kids

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CONSULTANT WHERE QUALITY MATTERS

Quality, efficiency and innovation are my main drivers. I started my passion for electronics as a teenager, loving to solve technical problems with engineering. I created methodologies for hunting complex bugs and used soft skills to build engaged teams. Spiced with a growth mindset targeting most complex and subtle bugs before design goes into production.
I am looking to engage with a company which targets quality, long term reusable methodologies, and which understand that taking care of Empoyees is the best way to get things done.

FREELANCE ACTIVITIES

06-2024 - ...

MyoAlert CONTACTEUR MUSCULAIRE

Founder https://myoalert.com/
Create and sell electronic devices to help disabled people to communicate.

Optimisez VOUS

Coach and trainer https://www.OptimisezVous.com
Focus on communication skills, leadership, decision making, well being.

DV++ METHODOLOGY

Consultant for verification methodologies, where quality matters.

codasip — VILLEUNEUVE LOUBET - FRANCE

2020 - 06-2024 **Director of Verification**

Create the French Design Center and recruit the first team members.
Main Challenge: **Grow the verification mindset in IP teams, delivering RISC-V processor IPs. Raise quality of verification to deliver to highest standards**.
Mentor engineers to raise awareness on quality, and how rare some bugs are.
Recruiting in Spain, France, Czech Republic, UK, Poland, from Junior to 20+ years experience.
Share best practice toward verification methodologies, **bringing shorter development time without sacrifying quality.**
Wrote blog articles 1 2 3 4, papers and speaker at conferences (DVCon 2022, Osmosis, Siemens U2U)
- Documentation templates, from verification plan to errata notice
- Enhance bug tracking and customer response

Brough up dedicated team for formal testing.
Drove different teams responsible for:
- Deliver random program generator
- Compute farm creation, job scheduling and monitoring
- Maintain and extend internal RISC-V architectural compliance test suite
- Develop accurate architectural checker
- Creating multiported memory agents (AXI, AHB)
- Various block level test benches (Coherent data cache, FPU, top level, MMU)

Engage with EDA vendors

arm — SOPHIA ANTIPOLIS - FRANCE

2019 - 2020 **Verification Lead for next M-Class CPU**
Challenge is fast delivery of a new technology
Choose the best methodologies, plan activity, set up team and resources

2017 - 2019 **Unit Level Verification Architect**.
Define methodologies to deliver faster the next generation A-class CPU.
Support team on transition of methodology.
Help transition to management for young leads
Chair on different internal verification related forums

2018 **Responsible for intern recruitment season**.
Set up the team of 3 leads and 15+ enginer-recruiters.
Train recruitment skills and delegation. Follow progress within the short timeframe.
Coach new intern's managers. 14 interns recruited this year.

2018 - … **Machine Learning tools for improving the verification**.
Experiment new algorithms to improve quality of constrain random generation.
Develop tools to automatically provide data and enhance model with Machine Learning team.

2016 - 2017 **Cortex-M23 verification** team member.
Assigned in the middle of the project to help recover delays in delivery.
Assess the current status of verification, change methodologies and priorities to help team deliver in time with the expected quality.

2013 - 2016 **Lead Memory System RIS tool development**.
Prototype started in 2010. Now used by CPU teams in 3 design centers.
Ensure team growth, customer support, and feature development toward finding difficult bugs.
Enhance FPGA-oriented algorithm for faster verification.
Today one of the main Verification tool for all A class CPUs.

2013 - 2014 **Cortex-A17 Verification Lead**
Track plan and activities towards all verification activities (top level, units level, system level).

2012 -… Member of **recruitment team for Verification and Design engineers**.
From interns to experienced, more that 100 interviews passed.
Mentor verification engineers for interview skills.

2012 - 2013 **Cortex-A12 Memory System Verification Lead**
Enhance test bench for **big.LITTLE** by generating more complex scenarios.
Co-develop tools needed for **new coverage metric**. Helps **improve test bench quality** when traditional coverage methodologies have saturated.

2012 - 2013 **Cortex-R8 Memory System Verification Lead**
Develop models and methodologies for verifying ECC error correction and detection.

2011 - 2012 **Cortex-A9 MPCore Maturity**
Introduce **Continuous Integration flow for RTL development** (Buildbot). Now used by all CPU teams (bamboo and Jenkins)
Start knowledge sharing teams for memory sub-system, in all 3 design centers
Document internal verification processes for arm CPUs.

2009 - 2010 **Cortex-R7 Memory System verification owner**
Enhance the strategy for MP verification. Develop drivers and checkers
1 patent filled
Introduce git in Sophia CPU teams for RTL development. Deploy the tool, train the team and support. Now git is the tool of choice for all arm RTL.

2008-2009 **Cortex-A9 MPCore L1 memory system test bench owner**
Define internal **memory system verification strategy** for Sophia MP CPUs. Still used today in 2 A class CPUs in Sophia and Cambridge.
Invent and develop **efficient regression tool** for unit test benches. Currently developed by a ~10 people team, used by most Cambridge and Sophia teams.

2006-2008 **Cortex-A9 MPCore memory system designer**
RTL design, validation and synthesis. Develop cycle accurate systemC model.
develop strategy for memory system multi unit test bench, improving existing BFMs, generators and checkers to support coherent multi-core CPU.
4 patents filled

2005-2006 **Cortex-R4 Bus Interface Unit verification**
Develop BFMs for AXI bus and RTL debug.
3 patents filled

2005 **ARM11 MPCore Test chip design and verification**
Develop and verify the bus matrix.

2004 **ARM1176JZ(F)-S Data Side verification**
Enhance test benches to support TrustZone and AXI protocol.

2003 **SecurCore SC100 team**
Wrote production tests in assembly

2002 **ARM7TDMI-S Rev4**
Verification automation

2002 **AES cryptography cipher**
6 month internship. Design, verify, implement AES cryptography cipher in hardware

Studies

2000 **SAGEM**, Paris. 6 weeks **intership**. Internal Database automation for electronic circuits

1999 - 2002 IMT Atlantique (was Télécom Bretagne) school master degree.

1997 - 1999 Lycée Marcelin Berthelot (Saint Maur) **Preparatory courses**

1997 High-School Degree with honors

Sides

2018, 2024 **President of Coach Around The World Sud Association**.
Offer personal coaching as charity
Grow the organisation and organise coaching training sessions with 15 participants.

since 2018 **Public speaking**
Conferences in Geneva and Cannes in 2018, Monaco and Cannes in 2019.
Topics related to personal development.

2008 Develop **robot for Eurobot competition** in a team of 3
Ending in 8th finals with 150 participants.
Responsible for electronic and firmware, using Atmel AVR connected to PDA and I²C sub-modules.

Skills

Programming: Python, C, C++, bash
Tools: Gitlab, Jenkins, Git, SVN, GNU/Linux, Docker, Grafana, Slurm, LFS, DevOps
ASIC design: Verilog, SystemC, systemVerilog assertions, EDA tools
Communication: Public speaking, coaching, mentoring, NLP, Non Violent Communication
Toys: ESP32/8266, Arduino, STM32, Raspberry Pi, Eagle PCB design, home automation
Language: French, English
Fun: Skiing, flying